

## FAULT TOLERANT STATIC TIMING ANALYSIS

### ABSTRACT

A method and system for performing fault tolerant static timing analysis for an electronic network. A composite timing graph is generated by making  $K + 1$  copies of the zero-defect timing graph of the network, where  $K$  is a predetermined maximum number of defects present on a path of the network, and static timing analysis is performed on the composite timing graph.

5

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